![ANALOG DEVICES]

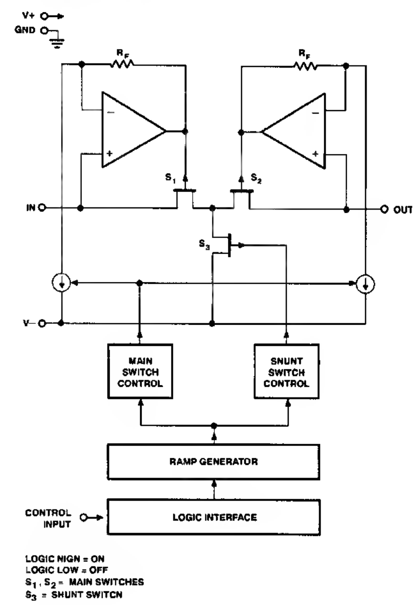
Dual Audio Analog Switches

SSM2402/SSM2412

FEATURES

- **"Clickless" Bilateral Audio Switching**
- **Guaranteed "Break-Before-Make" Switching**
- **Low Distortion: 0.003% typ**
- **Low Noise: 1 nV/$\sqrt{Hz}$**
- **Superb OFF-Isolation: 120 dB typ**
- **Low ON-Resistance: 60 Ω typ**
- **Wide Signal Range: $V_S = \pm 18$ V; 10 V rms**
- **Wide Power Supply Range: ±20 V max**
- **Available in Dice Form**

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The SSM2402/SSM2412 are dual analog switches designed specifically for high performance audio applications. Distortion and noise are negligible over the full audio operating range of 20 Hz to 20 kHz at signal levels of up to 10 V rms. The SSM2402/SSM2412 offer a monolithic integrated alternative to expensive and noisy relays or complex discrete JFET circuits. Unlike conventional general-purpose CMOS switches, the SSM2402/SSM2412 provide superb fidelity without audio "clicks" during switching.

Conventional TTL or CMOS logic can be used to control the switch state. No external pull-up resistors are needed. A "T" configuration provides superb OFF-isolation and true bilateral operation. The analog inputs and outputs are protected against overload and overvoltage.

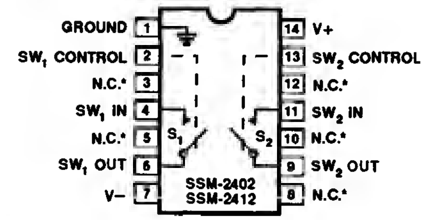
An important feature is the guaranteed "break-before-make" for all units, even IC-to-IC. In large systems with multiple switching channels, all separate switching units must open before any switch goes into the ON-state. With the SSM2402/SSM2412, you can be certain that multiple circuits will all break-before-make.

The SSM2402/SSM2412 represent a significant step forward in audio switching technology. Distortion and switching noise are significantly reduced in the new SSM2402/SSM2412 bipolar-JFET switches relative to CMOS switching technology. Based on a new circuit topology that optimizes audio performance, the SSM2402/SSM2412 make use of a proprietary bipolar-JFET process with thin-film resistor network capability. Nitride capacitors, which are very area efficient, are used for the proprietary ramp generator that controls the switch resistance transition. Very wide bandwidth amplifiers control the gate-to-source voltage over the full audio operating range for each switch. The ON-resistance remains constant with changes in signal amplitude and frequency, thus distortion is very low, less than 0.01% max.

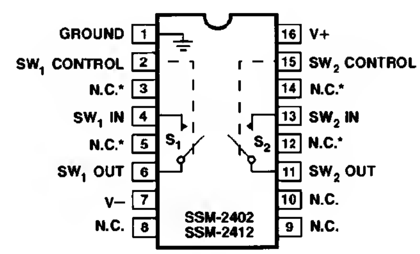
The SSM2402 is the first analog switch truly optimized for high-performance audio applications. For broadcasting and other switching applications which require a faster switching time, we recommend the SSM2412—a dual analog switch with one-third of the switching time of the SSM2402.

PIN CONNECTIONS

14-Pin Epoxy DIP (P-Suffix)



16-Pin SOL (S-Suffix)



* GUARD PINS FOR INPUT/OUTPUT ISOLATION (GROUND FOR BEST PERFORMANCE)

REV. A

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Tel: 617/329-4700 Fax: 617/326-8703

SSM2402/SSM2412–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±18 V, R_L = OPEN, and –40°C ≤ T_A ≤ +85°C unless otherwise noted. All specifications, tables, graphs, and application data apply to both the SSM2402 and SSM2412, unless otherwise noted.)

Parameter	Symbol	Conditions	SSM2402/SSM2412 Min	Typ	Max	Units
POSITIVE SUPPLY CURRENT	$+I_{SY}$	V_{IL} = 0.8 V, 2.0 V[1]		6.0	7.5	mA
NEGATIVE SUPPLY CURRENT	$-I_{SY}$	V_{IL} = 0.8 V, 2.0 V[1]		4.8	6.0	mA
GROUND CURRENT	I_{GND}	V_{IL} = 0.8 V, 2.0 V[1]		0.6	1.5	mA
DIGITAL INPUT HIGH	V_{INH}	T_A = Full Temperature Range	20			V
DIGITAL INPUT LOW	V_{INL}	T_A = Full Temperature Range			0.8	V
LOGIC INPUT CURRENT	I_{LOGIC}	V_{IN} = 0 V to 15 V[2]		1.0	5.0	μA
ANALOG VOLTAGE RANGE[3]	V_{ANALOG}		–14.2		+14.2	V
ANALOG CURRENT RANGE[3]	I_{ANALOG}		–10		+10	mA
OVERVOLTAGE INPUT CURRENT		V_{IN} = ±V_{SUPPLY}		±40		mA
SWITCH ON RESISTANCE	R_{ON}	–14.2 V ≤ V_A ≤ +14.2 V I_A = ±10 mA, V_{IL} = 2.0 V T_A = +25°C T_A = Full Temperature Range Tempco ($\Delta R_{ON}/\Delta T$)		 60 0.2	 85 115	 Ω Ω Ω/°C
R_{ON} MATCH	R_{ON} MATCH	–14.2 V ≤ V_A ≤ +14.2 V I_A = ±10 mA, V_{IL} = 2.0 V		1	5	%
SWITCH ON LEAKAGE CURRENT	$I_{S(ON)}$	V_{IL} = 2.0 V –14.2 V ≤ V_A ≤ +14.2 V V_A = 0 V		 0.05 0.05	 1.0 10.0	 μA nA
SWITCH OFF LEAKAGE CURRENT	$I_{S(OFF)}$	V_{IL} = 0.8 V –14.2 V ≤ V_A ≤ +14.2 V V_A = 0 V		 0.05 0.05	 1.0 10.0	 μA nA
TURN-ON TIME[4]	t_{ON}	V_A = +10 V, R_L = 2 kΩ SSM2402 T_A = +25°C, See Test Circuit SSM2412		10.0 3.5		ms
TURN-OFF TIME[5]	t_{OFF}	V_A = +10 V, R_L = 2 kΩ SSM2402 T_A = +25°C, See Test Circuit SSM2412		4.0 1.5		ms
BREAK-BEFORE-MAKE TIME DELAY[6]	$t_{OFF}-t_{ON}$	T_A = +25°C SSM2402 SSM2412		6.0 2.0		ms
CHARGE INJECTION	Q	T_A = +25°C SSM2402 SSM2412		50 150		pC
ON-STATE INPUT CAPACITANCE	$CS_{(ON)}$	V_A = 1 V rms f = 5 kHz, T_A = +25°C		12		pF
OFF-STATE INPUT CAPACITANCE	$CS_{(OFF)}$	V_A = 1 V rms f = 5 kHz, T_A = +25°C		4		pF
OFF ISOLATION	$I_{SO(OFF)}$	V_A = 10 V rms, 20 Hz to 20 kHz T_A = +25°C, See Test Circuit		120		dB
CHANNEL-TO-CHANNEL CROSSTALK	C_T	V_A = 10 V rms, 20 Hz to 20 kHz T_A = +25°C		96		dB
TOTAL HARMONIC DISTORTION[7]	THD	0 V to 10 V rms, 20 Hz to 20 kHz T_A = +25°C, R_L = 5 kΩ		0.003	0.01	%
SPECTRAL NOISE DENSITY	e_n	20 Hz to 20 kHz, T_A = +25°C		1		nV/$\sqrt{Hz}$
WIDEBAND NOISE DENSITY	e_n p-p	20 Hz to 20 kHz, T_A = +25°C		0.2		μV p-p

NOTES
[1]"V_{IL}" is the Logic Control Input.
[2]Current tested at V_{IN} = 0 V. This is the worst case condition.
[3]Guaranteed by R_{ON} test condition.
[4]Turn-ON time is measured from the time the logic input reaches the 50% point to the time the output reaches 50% of the final value.
[5]Turn-OFF time is measured from the time the logic input reaches the 50% point to the time the output reaches 50% of the initial value.
[6]Switch is guaranteed by design to provide break-before-make operation.
[7]THD guaranteed by design and dynamic R_{ON} testing.

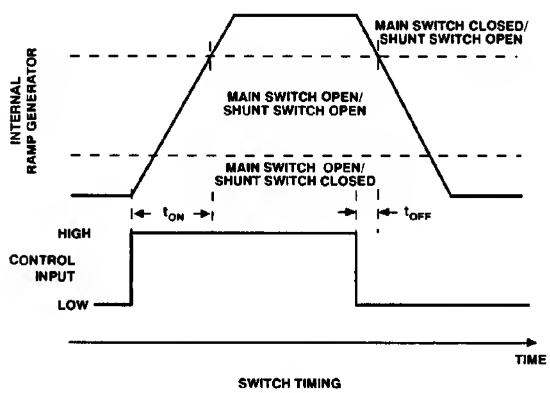
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range . . . . –40°C to +85°C
Operating Supply Voltage Range . . . . ±20 V
Analog Input Voltage Range
Continuous . . . . $V- +3.5\ V \le V_A \le V+ -3.5\ V$
Maximum Current Through Switch . . . . 20 mA
Logic Input Voltage Range . . . . V+ Supply to –2 V
V+ Supply to Ground . . . . +36 V
V– Supply to Ground . . . . –20 V
V_A to V– Supply . . . . +36 V

Package Type	θ_{JA}*	θ_{JC}	Units
14-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SOL (S)	92	27	°C/W

*θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for P-DIP package; θ_{JA} is specified for device soldered to printed circuit board for SOL package.



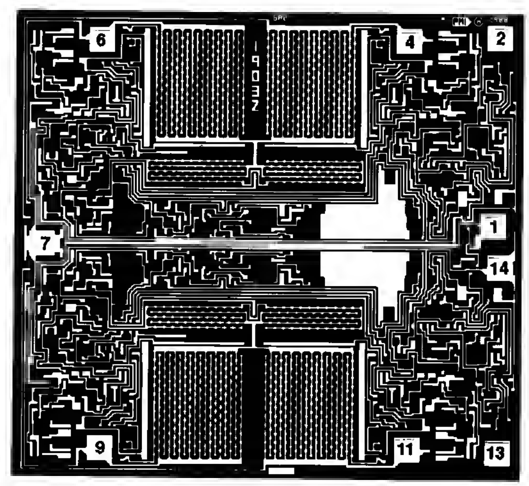
Timing Diagram

ORDERING GUIDE

Model	Temperature Range	Package Description
SSM2402P	–40°C to +85°C	14-Pin Plastic DIP
SSM2402S	–40°C to +85°C	16-Pin SOL
SSM2412P	–40°C to +85°C	14-Pin Plastic DIP
SSM2412S	–40°C to +85°C	16-Pin SOL

DICE CHARACTERISTICS

Die Size 0.105 × 0.097 Inch, 10,185 sq. mils
(2.667 × 2.464 mm, 6.57 sq. mm)

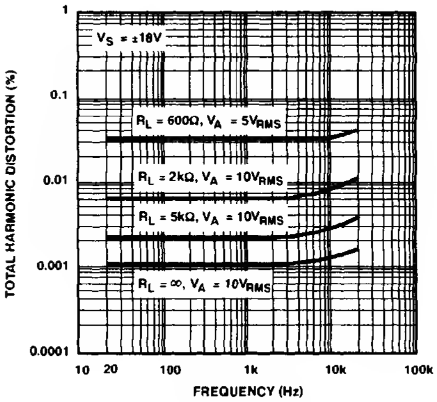


WAFER TEST LIMITS

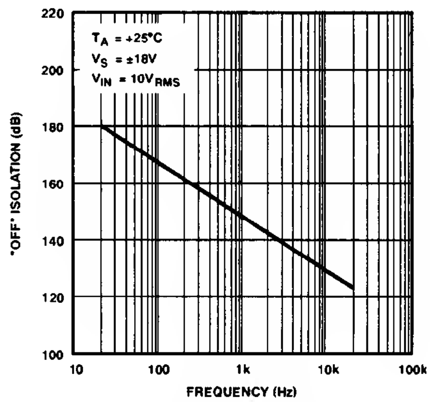
Parameter	Symbol	Conditions[1]	Limit	Units
POSITIVE SUPPLY CURRENT	$+I_{SY}$	$V_{IL} = 0.8$ V	7.5	mA max
NEGATIVE SUPPLY CURRENT	$-I_{SY}$	$V_{IL} = 0.8$ V	6.0	mA max
GROUND CURRENT	I_{GND}	$V_{IL} = 0.8$ V	1.5	mA max
LOGIC INPUT CURRENT	I_{LOGIC}	$V_{IN} = 0$ V[2]	5.0	µA max
SWITCH ON RESISTANCE	R_{ON}	$-14.2\ V \le V_A \le +14.2\ V$ $I_A = \pm 10$ mA, $V_{IL} = 2.0$ V	85	Ω max
R_{ON} MATCH BETWEEN SWITCHES	R_{ON} MATCH	$-14.2\ V \le V_A \le +14.2\ V$ $I_A = \pm 10$ mA, $V_{IL} = 2.0$ V	5	% max
SWITCH ON LEAKAGE CURRENT	$I_{S(ON)}$	$-14.2\ V \le V_A \le +14.2\ V$, $V_{IL} = 2.0$ V	1.0	µA max
SWITCH OFF LEAKAGE CURRENT	$I_{S(OFF)}$	$-14.2\ V \le V_A \le +14.2\ V$, $V_{IL} = 0.8$ V	1.0	µA max

NOTES
[1]V_{IL} = Logic Control Input; V_A = Applied Analog Input Voltage; I_A = Applied Analog Input Current.
[2]Worst Case Condition.
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

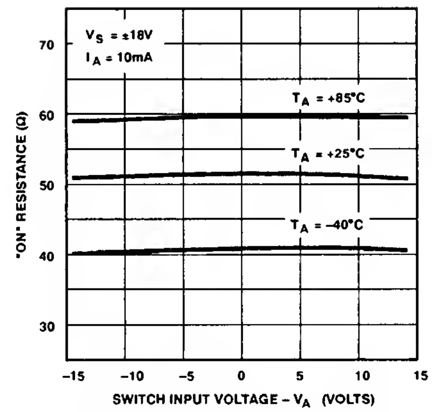
SSM2402/SSM2412- Typical Performance Characteristics



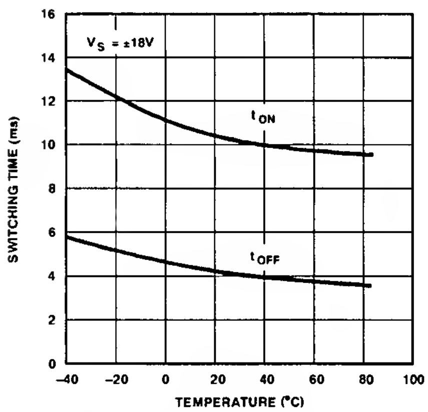
Total Harmonic Distortion vs. Frequency



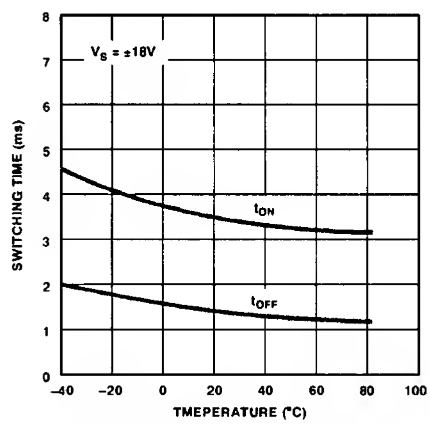
"OFF" Isolation vs. Frequency



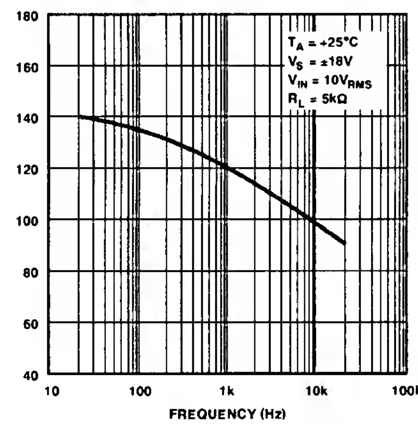
"ON" Resistance vs. Analog Voltage



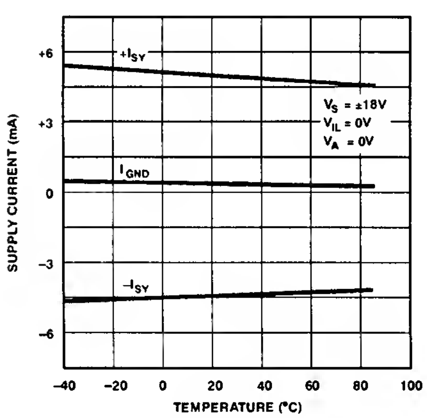
SSM2402 Switching Time vs. Temperature



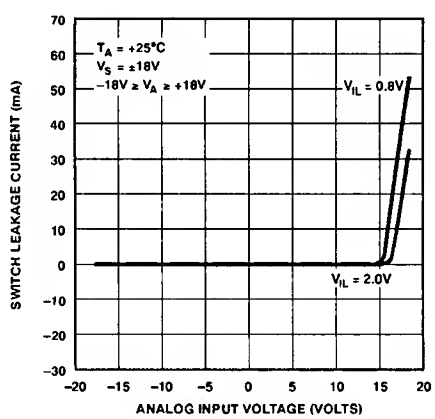
SSM2412 Switching Time vs. Temperature



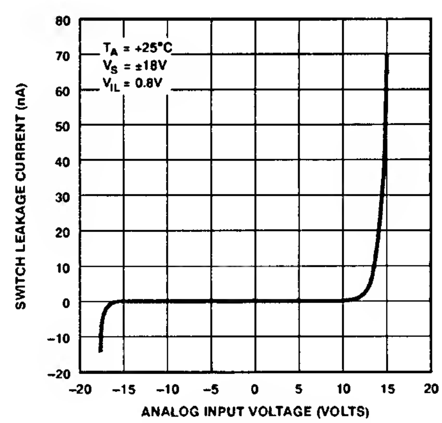
Channel Separation vs. Frequency



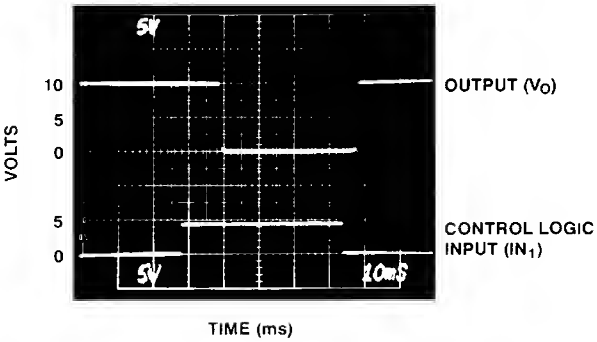
Supply Current vs. Temperature



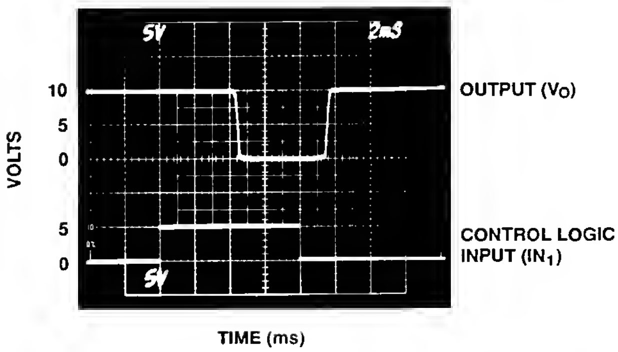
Overvoltage Characteristics



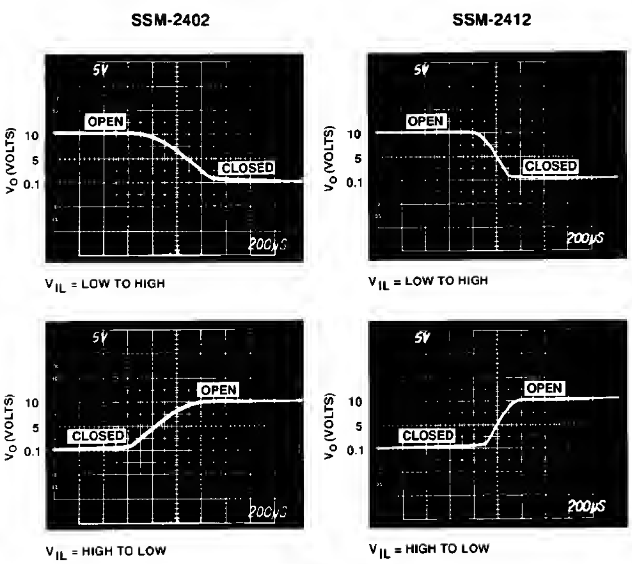
Leakage Current vs. Analog Voltage



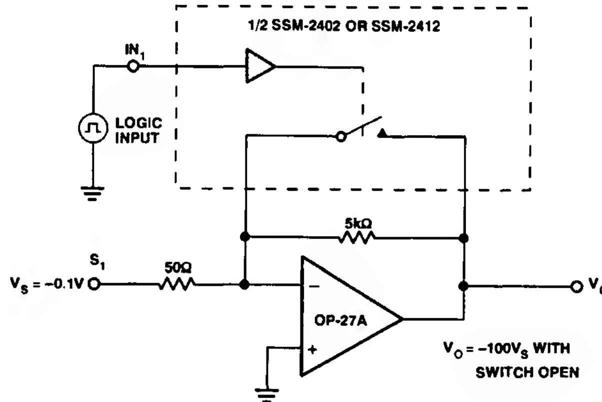
SSM2402 T_{ON}/T_{OFF} Switching Response



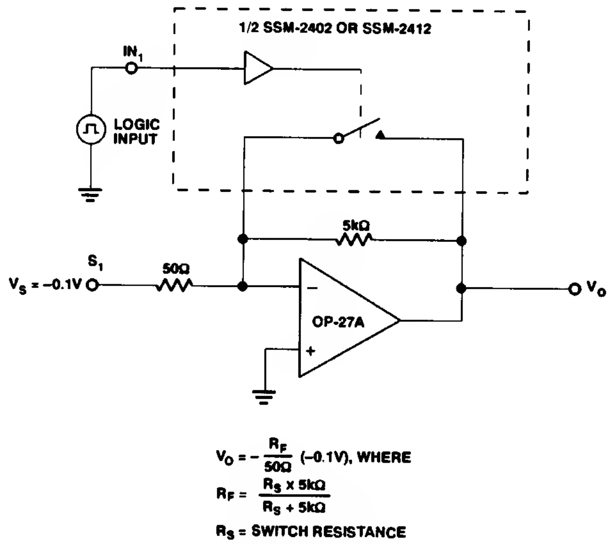
SSM 2412 T_{ON}/T_{OFF} Switching Response



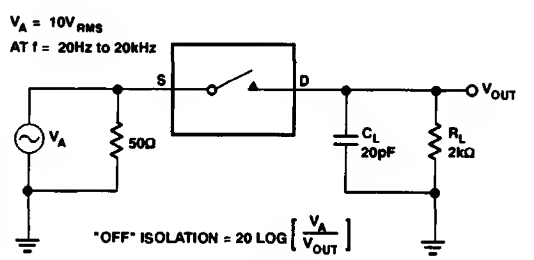
Switching ON/OFF Transition



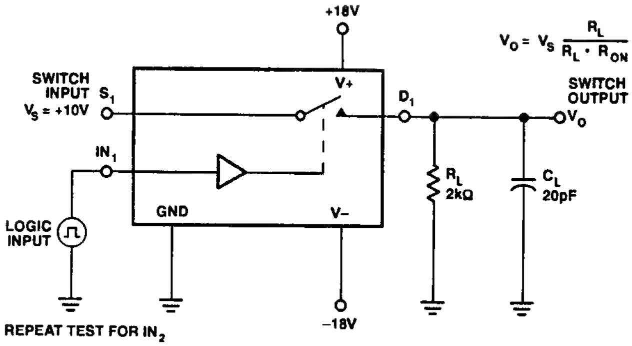
T_{ON}/T_{OFF} Switching Response Test Circuit

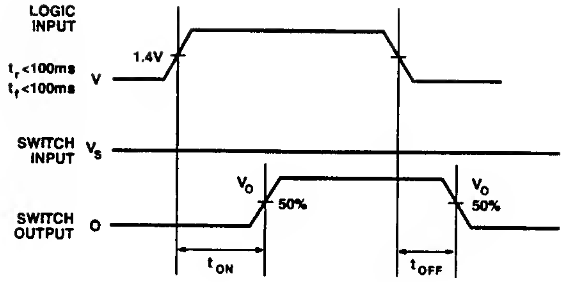


Switch ON/OFF Transition Test Circuit

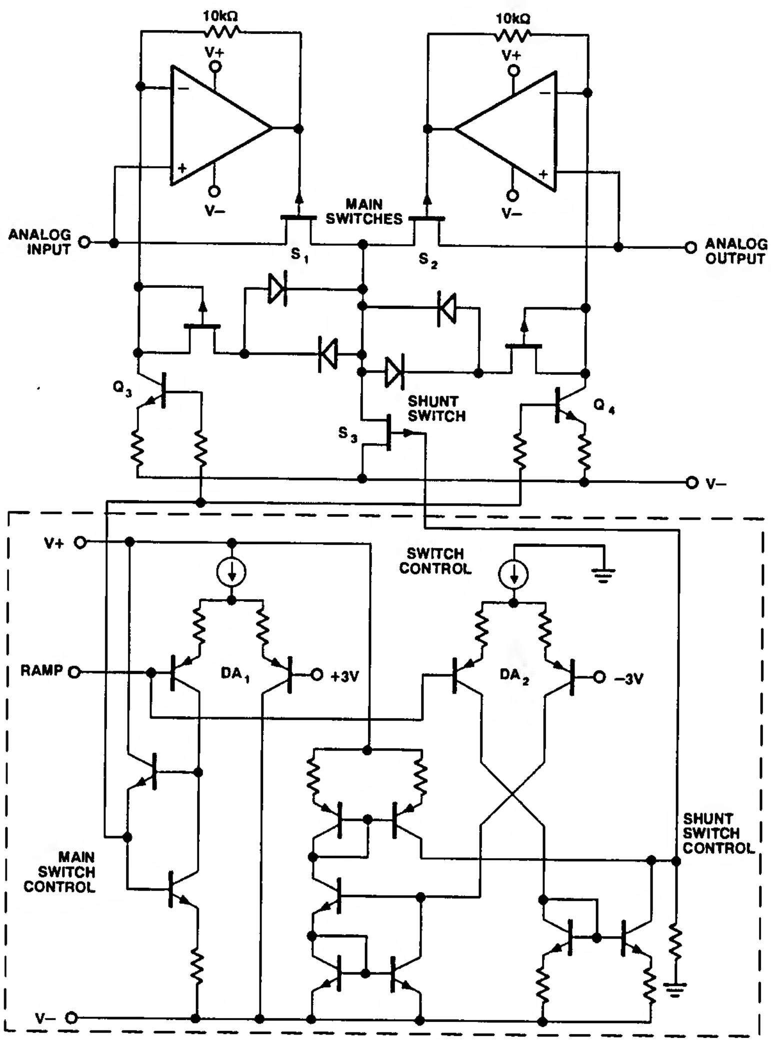


"OFF" Isolation Test Circuit





Switching Time Test Circuit



Simplified Schematic

APPLICATIONS INFORMATION

FUNCTIONAL SECTIONS

Each half of the SSM2402/SSM2412 are made up of three major functional blocks:

1. **"T" Switch**
   Consists of JFET switches S_1 and S_2 in series as the main switches and switch S_3 as a shunt.
2. **Ramp Generator**
   Generates a ramp voltage on command of the Control Input (see Figure 1). A LOW-to-HIGH TTL input at Control Input initiates a ramp that goes from approximately –7 V to +7 V in 12 ms. Conversely, a HIGH-to-LOW TTL transition at Control Input will cause a downward ramp from approximately +7 V to –7 V in 12 ms for the SSM2402, and 4 ms for the SSM2412. The Ramp Generator also supplies the +3 V and –3 V reference levels for Switch Control.
3. **Switch Control**
   The ramp from the Ramp Generator section is applied to two differential amplifiers (DA_1 and DA_2) in the Switch Control block. (See Simplified Schematic). One amplifier is referenced to –3 V and the other is referenced to +3 V. Switch Control Outputs are:
   - **Main Switch Control**—Drives two 0.25 mA current sources that control the inverting inputs of each op amp. When ON, the current sources cause a gate-to-source voltage of approximately 2.5 V which is sufficient to turn off S_1 and S_2. When the current sources from Main Switch Control are OFF, each op amp acts as a unity-gain follower (V_{GS} = 0) and both switches (S_1 and S_2) will be ON.
   - **Shunt Switch Control**—Controls the Shunt Switch of the "T" configuration.

SWITCH OPERATION

Unlike conventional analog switches, the SSM2402/SSM2412 are designed to ramp on and off gradually over several milliseconds. The soft transition prevents popping or clicking in audio systems. Transients are minimized in active filters when the SSM2402/SSM2412 are used to switch component values.

To see how the SSM2402/SSM2412 switches work, first consider an OFF-to-ON transition. The Control Input is initially LOW and the Ramp Output is at approximately –7 V. The Main Switch Control is HIGH which drives current sources Q_3 and Q_4 to 0.25 mA each. These currents generate 2.5 V gate-to-source back bias for each JFET switch (S_1 and S_2) which holds them OFF.

The Shunt Switch Control is negative which holds the shunt JFET S_3 ON. Undesired feedthrough signals in the series JFET switches S_1 and S_2 are shunted to the negative supply rail through S_3.

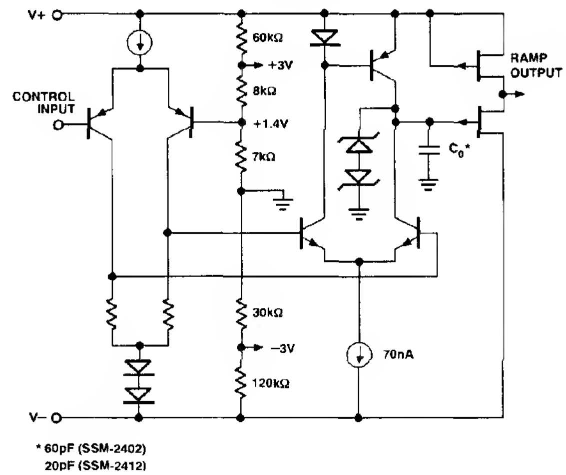


Figure 1. Ramp Generator

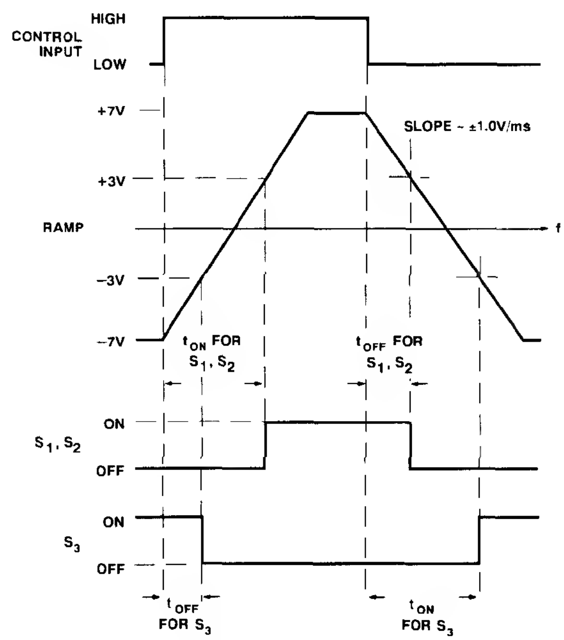


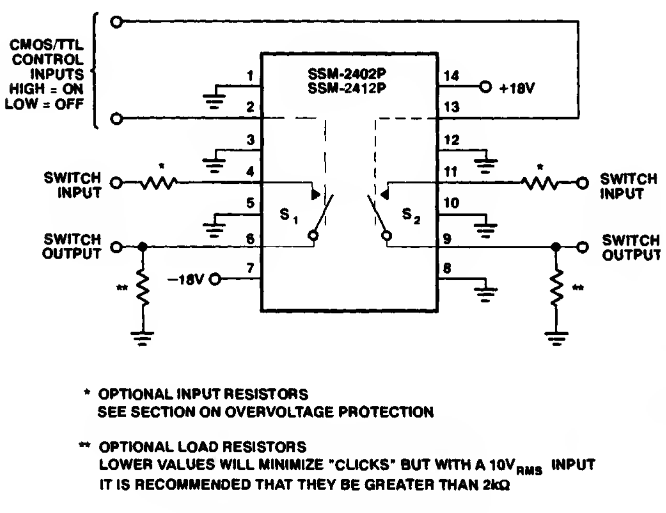
Figure 2. Switch Control

When the Control Input goes from LOW to HIGH, the Ramp Generator slews in the positive direction as shown in Figure 2. When the ramp goes more positive than –3 V, the Shunt Switch Control is pulled positive by differential amplifier DA_2 which thereby puts shunt switch S_3 into the OFF state. Note that S_1 and S_2 are still OFF, so at this time all three switches in the "T" are OFF.

When the Ramp Output reaches +3 V, and the drive for the Main Switch Control output is gated OFF by differential amplifier DA_1, current sources Q_3 and Q_4 go to the OFF state and the V_{GS} of each main switch goes to zero. The high speed op amp followers provide essentially zero gate-to-source voltage over the full audio signal range; this in turn assures a constant low impedance in the ON state over the full audio signal range. Total time to turn on the SSM2402 switch is approximately 10.0 ms and 3.5 ms for the SSM2412.

In systems using a large number of separate switches, there are advantages to having faster switching into OFF state than into the ON state. Break-before-make can be maintained at the system level. To see how the SSM2402/SSM2412 guarantee break-before-make, consider the ON-to-OFF transition.

A Control Input LOW initiates the ON-to-OFF transition. The Ramp Generator integrates down from approximately +7 V towards –7 V. As the ramp goes through +3 V, the comparator controlling the Main Switches (S_1 and S_2) goes HIGH and turns on current sources Q_3 and Q_4 which thereby puts S_1 and S_2 into the OFF state. At this time, all switches in the "T" are OFF. When the ramp integrates down to –3 V, the Shunt Switch Control changes state and pulls shunt switch S_3 into the ON state. This completes the ON-to-OFF transition; S_1 and S_2 are OFF, and S_3 is ON to shunt away any undesired feedthrough. Note though that the ON-to-OFF time for main switches S_1 and S_2 is only the time interval required for the ramp to go from +7 V to +3 V, about 4 ms for the SSM2402, and 1.5 ms for the SSM2412. The time to turn on is about 2.5 times as long as the time to turn off.



Typical Configuration

The SSM2402/SSM2412 are much more than simple single solid state switches. The "T" configuration provides superb OFF-isolation through shunting of feedthrough via shunt switch S_3. Break-before-make is inherent in the design. The ramp provides a controlled gating action that softens the ON/OFF transitions. Distortion is minimized by holding zero gate-to-source voltage for the two main FET switches, S_1 and S_2, using the two op amp followers. Figure 3 shows a distortion comparison between the SSM2402 and a typical CMOS switch. In summary, the SSM2402/SSM2412 are designed specifically for high performance audio system usage.

OVERVOLTAGE PROTECTION

The SSM2402/SSM2412 are designed to guarantee correct operation with inputs of up to ±14.2 V with ±18 V supplies. The switch input should never be forced to go beyond the supply rails. In the OFF condition, if the inputs exceeds +14.2 V, there is a risk of turning the respective input pass FET "ON." When the input voltage rises to within 3.8 V of the positive supply, the op amp follower saturates and will not be able to maintain the full 2.5 V of back bias on the gate-to-source junction. Under this condition, current will flow from the input through the shunt FET to the negative supply. This current is substantial, but is limited by the FET I_{DSS}. Although this current will not damage the device, there is a danger of also turning on the output pass FET, especially if the output is close to the negative rail.

This risk of signal "breakthrough" for inputs above +14.2 V can be eliminated by using a source resistor of 100 Ω–500 Ω in series with the analog input to provide additional current limiting.

Near the negative supply, transistors Q_3 and Q_4 saturate and can no longer keep the switch OFF. Signal breakthrough cannot happen, but the danger here is latch-up via a path to V– through the shunt FET. Additional circuitry (not shown) has been incorporated to turn OFF the shunt FET under these conditions, and the potential for latch-up is thereby eliminated.

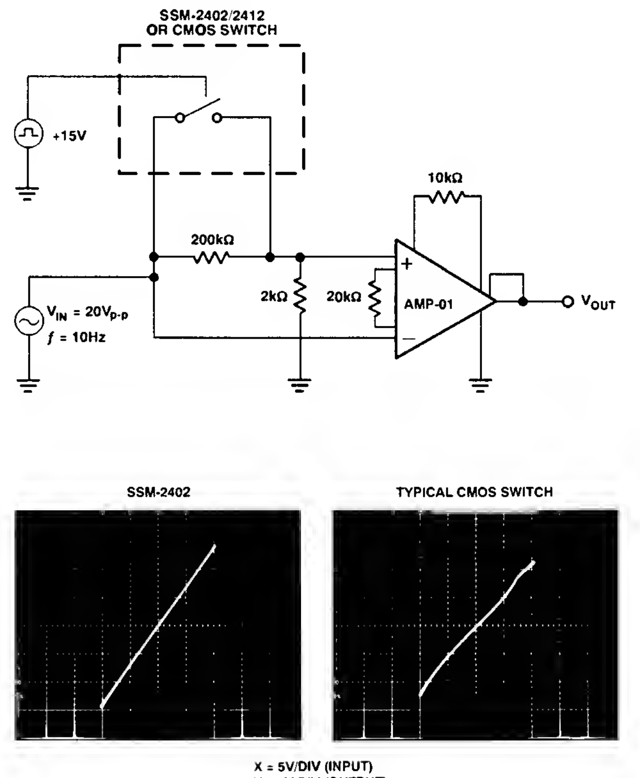


Figure 3. Comparison of the SSM2402 and Typical CMOS Switch for Distortion

DIGITALLY-CONTROLLED ATTENUATOR

Figure 4 shows the usual approach to digitally-controlled attenuation. With S_1 closed, the signal passes unattenuated to the output. With S_1 open and S_2 closed, the signal is attenuated by R_1 and R_2. The advantage of this configuration is that the attenuator current does not have to flow through the switches. The disadvantage is that the output is undefined during the switching period, which can be several milliseconds.

The low distortion characteristics of the SSM2402/SSM2412 enable the alternate arrangement of Figure 5 to be used. Now only one switch is required to change between two gains, and there is always a signal path to the output. Values for R_2 will typically be in the low kilohm range.

For more gain steps and higher attenuation, the ladder arrangement of Figure 6 can be used. This enables a wide dynamic range to be achieved without the need for large value resistors, which would result in degradation of the noise performance.

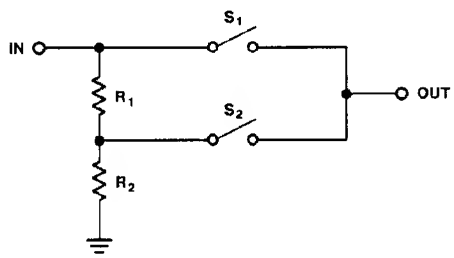


Figure 4.

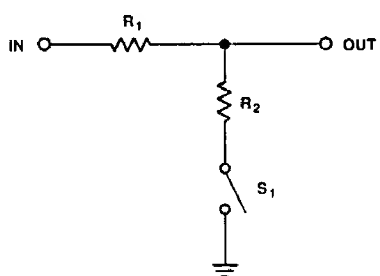


Figure 5.

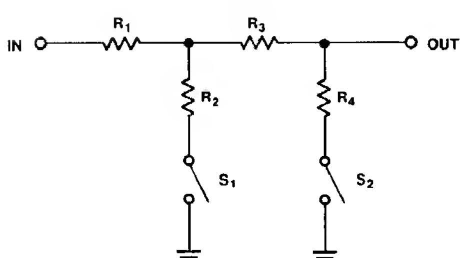


Figure 6.

HIGH PERFORMANCE STEREO ROUTING SWITCHER

The SSM2402 Dual Audio Switch comprises the nucleus for this 16 channels-to-one high performance stereo audio routing switcher, which features negligible noise and low distortion over the frequency range of 20 Hz to 20 kHz. This performance is achieved even while driving 600 Ω loads at signal levels up to +30 dBu.

The SSM2402 affords a much simplified electrical design and printed circuit board layout, along with reduced manufacturing cost, when compared with discrete JFET circuits of similar performance. The electrical performance of the design described is vastly superior to CMOS switch designs, which are more prone to failure resulting from electrical static discharge.

The switching control of the SSM2402 may be activated by conventional mechanical switches or 5 volt TTL or CMOS logic circuits. The application shown utilizes a simple mechanical control switch for illustration purposes only. Many diverse X/Y control schemes, destination control, or computer controlled designs can be utilized.

The "T" configuration of the SSM2402 switch provides excellent ON-OFF isolation. The SSM2402 also features ms ramped turn on and ms ramped turn off for click-free switching. Additionally, the switch has a break-before-make switching sequence. Both features become significant in large audio switching systems where the audio path can pass through multiple switching elements. Such controlled switching is very important in large systems used in broadcast program switching or in production work.

The application circuit design also employs the SSM2015 balanced input amplifier (Figure 7). The input impedance is high (≈100 kΩ), balanced or unbalanced. The input circuit incorporates a single pole RFI filter with a cutoff frequency set at 145 kHz. In addition, the input circuit attenuates the signal by 25 dB and extends the common-mode input voltage range to ±98 volts peak, with common-mode rejection greater than 70 dB from 20 Hz to 20 kHz. The SSM2015 is set to produce a 15 dB gain. The signal drive level into the SSM2402 switch is then +10 dBu with a +20 dBu input level and +14 dBu peak, well within ideal operating range. Good signal-to-noise is maintained, with generous head-room available by electing to use ±18 V dc power supply voltages.

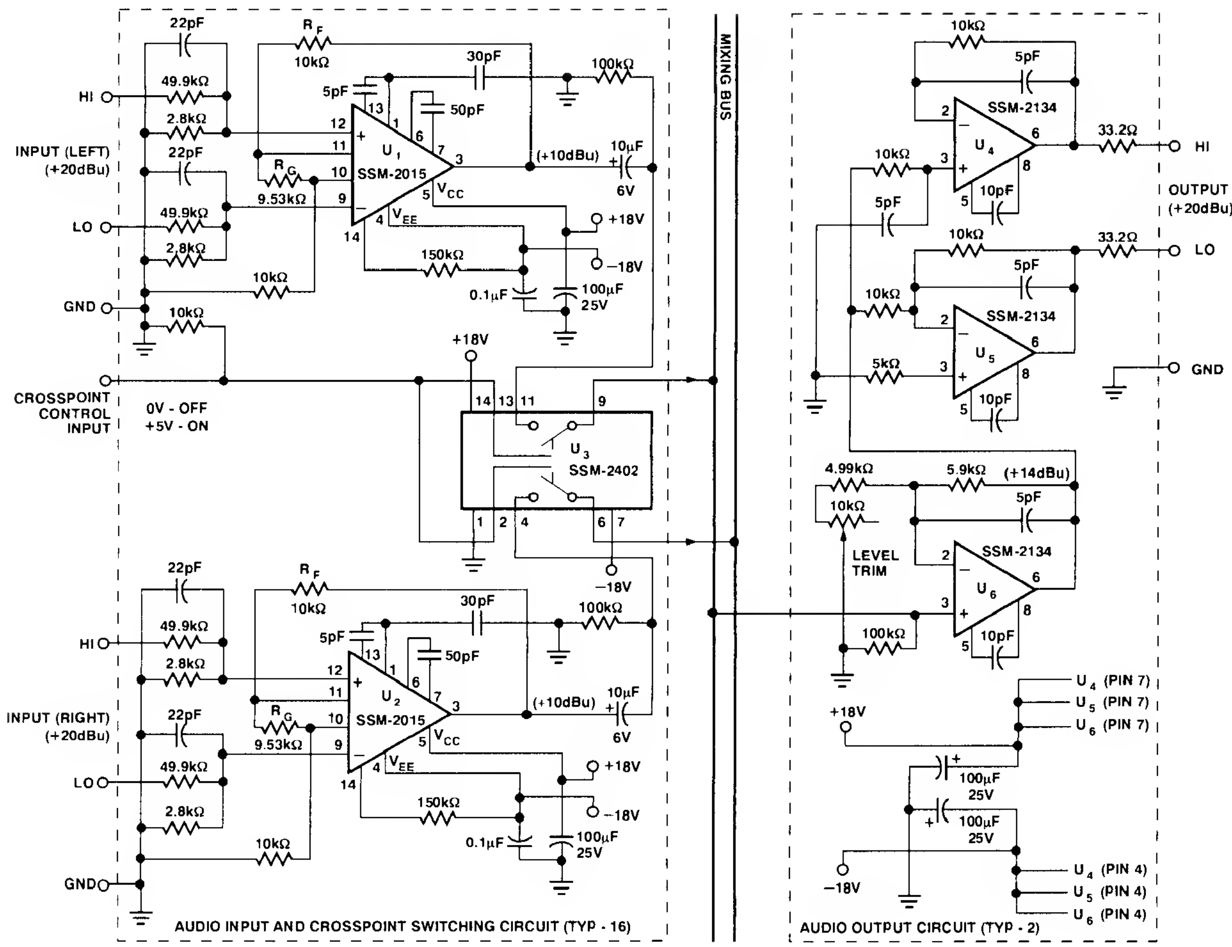


Figure 7. Switcher Schematic

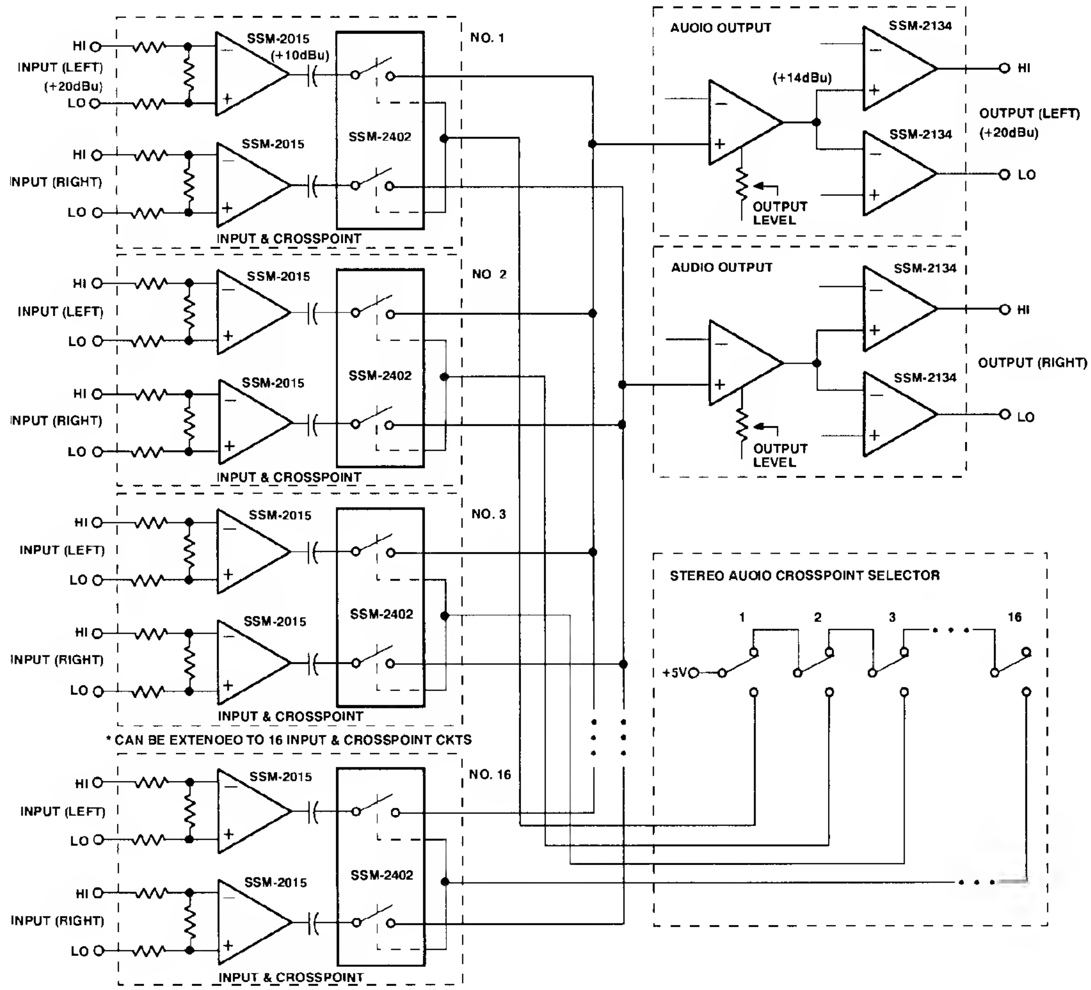


Figure 8. Switcher Functional Block Diagram

The routing switcher bus carries high level unbalanced audio, but is driven with low impedance sources. With the output impedance of the SSM 2015 at virtually 0 Ω and the SSM 2402 switch ON, resistance is typically 60 Ω. Bus-to-bus crosstalk is exceptionally low. For example, assuming 14 pF coupling between buses and 20 kHz signal, the crosstalk (isolation) exceeds 80 dB. The 14 pF would be representative for the 16 × 1 stereo design shown. Shielding of the buses with a printed circuit board ground plane and physically isolating the input and output circuits will reduce the crosstalk even further. The "T" configuration of the SSM 2402 switch virtually eliminates crosstalk between the various input signal sources.

The output amplifier incorporates a buffer amplifier that provides 4 dB of gain (nominally), with adjustable output level trim control. The buffer also isolates the switching bus from the balanced output amplifier circuit. The balanced output is designed to drive 600 Ω loads and utilizes two SSM 2134 IC amplifiers. The differential design increases drive capability, yet increases the heat dissipation surface area, and keeps IC package temperature well within safe operating limits, even when driving 600 Ω loads. The SSM 2134 is recommended due to its low noise, wide frequency response, and output drive current capabilities.

Overall performance of the 16 × 1 stereo switcher is noteworthy. Input-to-output frequency response is flat to within 1 dB over a 10 Hz to 50 kHz band. Total harmonic distortion plus noise is less than 0.03%, from 20 Hz to 20 kHz. SMPTE intermodulation distortion is less than 0.02%. The use of ±18 V dc power supplies produces a +30 dBm clip level, even when driving 600 Ω loads.

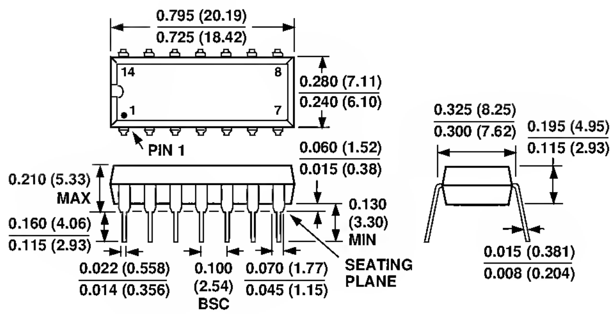
Table I. Circuit Performance Specifications

Max Input Level	+30 dBu
Input Impedance, Unbalanced	100 kΩ
Input Impedance, Balanced	200 kΩ
Common-Mode Rejection (20 Hz to 20 kHz)	>70 dB
Common-Mode Voltage Limit	±98 V Peak
Max Output Level	+30 dBu/dBm
Output Impedance	67 Ω
Gain Control Range	±2 dB
Output Voltage Slew Rate	6 V/µs
Frequency Response (±0.05 dB)	20 Hz to 20 kHz
Frequency Response (±0.5 dB)	10 Hz to 50 kHz
THD + Noise (20 Hz to 20 kHz, +8 dBu)	0.005%
THD + Noise (20 Hz to 20 kHz, +24 dBu)	0.03%
IMD (SMPTE 60 Hz & 4 kHz, 4:1, +24 dBu)	0.02%
Crosstalk (20 Hz to 20 kHz)	>80 dB
S/N Ratio @ 0 dB Gain	135 dB

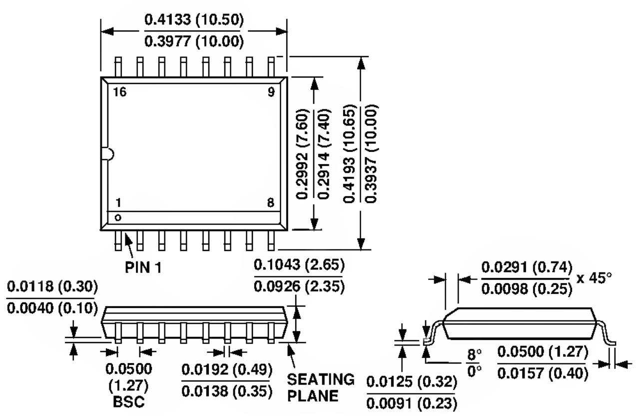
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

14-Pin Epoxy DIP (P-Suffix)



16-Pin SOL (S-Suffix)



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